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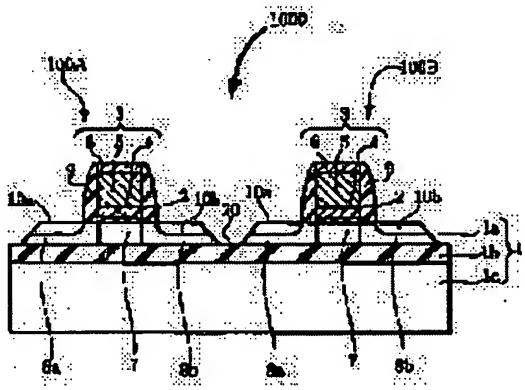
(54) SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device together with its manufacturing method for high current driving capacity and yield.

SOLUTION: A semiconductor device 1000 comprises an NMOSFET 100A and a PMOSFET 100B. Each MOSFET comprises first and second impurity diffusion layers 8a and 8b which are formed at a silicon layer 1a of an SOI substrate 1 and constitute a source region and a drain region, a channel region 7 formed between first and second impurity diffusion layers 8a and 8b, a gate insulating layer 2 formed at least on the channel region 7, and a gate electrode 3 formed on the gate insulating layer 2. The gate electrode 3 comprises a tantalum nitride layer 4 at least in a region contacting the gate insulating layer 2, and a tantalum layer 5 formed on the tantalum nitride layer 4. The tantalum layer 5 has a crystal structure comprising body-centered cubic lattice phase.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the insulated-gate field-effect transistor which has the description in a gate electrode, and its manufacture approach about a semiconductor device and its manufacture approach.
[0002]
[Background of the Invention] In the insulated-gate field-effect transistor (MISFET) used for a current semiconductor integrated circuit, the polycrystalline silicon layer which doped the impurity by high concentration for the reduction in resistance is used as the gate electrode in many cases. In the semi-conductor process used for a concrete CMOS circuit (Complimentary MOSFET circuit), in order to maintain property balance, as a gate electrode material, N type polycrystalline silicon is adopted as N-channel metal oxide semiconductor FET (NMOSFET), and P type polycrystalline silicon is adopted as P channel MOSFET (PMOSFET). Moreover, as for a gate electrode, it is common to take the structure of having a refractory metal silicide layer in the upper layer of said gate electrode for the purpose of the further reduction in resistance.
[0003] However, causing depletion-ization is known although the polish recon layer which constitutes a gate electrode has doped the impurity by high concentration. If depletion-ization occurs, it will become that capacity is inserted in a gate electrode and a serial, and equivalence, and the effectual electric field concerning a channel will fall. Consequently, the current drive capacity of MOSFET declines. Moreover, the resistance of the whole gate electrode is difficult for carrying out to below 5ohms / **, even when a silicide layer is piled up on a polycrystalline silicon layer. And if even a 0.1-micron generation makes a device detailed, since it is necessary to make thickness of a gate electrode thin, making a gate electrode below into 30micro ohm-cm extent at the rate of specific resistance is called for.
[0004] On the other hand, the work function of the N type polycrystalline silicon layer which touches a direct gate insulating layer is 5.25eV, and the work function of 4.15eV and a P type polycrystalline silicon layer serves as [these work functions] value [eV / of silicon / intrinsic mid gap energy 4.61] greatly shifted. This big difference brings about increase of the absolute value of flat band voltage VFB in the MOS capacitor made with a metal-insulating-layer-semi-conductor (signs differ by NMOSFET and PMOSFET). Therefore, it is necessary to shift the optimum value of the high impurity concentration in a channel to a high concentration side for the purpose of control of a threshold VTH in such an MOSFET. And within a high-concentration channel, the effect which cannot disregard dispersion of the carrier by the impurity will be done, consequently the fall of the carrier mobility in a channel will be caused. This means the fall of the current drive capacity of MOSFET, and does effect important for the response characteristic of a circuit.
[0005] In order to solve these troubles, the gate electrode material which does not cause gate

depletion-ization by low resistance, and has various work functions is proposed. For example, Jeong-Mo At Hwang (IEDM Technical Digest 1992, 345 pages), the structure which used the beta tantalum (beta-Ta) layer (IEDM Technical Digest 1996, 117 pages) is proposed by the structure which used the titanium nitride (TiN) layer, and ****.

[0006] For example, in N type or P-channel MOS FET, the following things can say about the gate electrode which has the TiN layer formed on the gate insulating layer. Since a TiN layer has the rate of specific resistance comparatively as high as about 200micro ohm-cm, the laminating of the metal (for example, tungsten) layer is carried out for the reduction in resistance of a gate electrode. As it is also in the report of Jeong-Mo Hwang etc., 4.7-4.8eV and intrinsic mid gap energy 4.61eV of silicon are expected by the work function of a TiN layer that near and big effectiveness are acquired in respect of the threshold control mentioned above.

[0007] However, in this example of a configuration, since it dissolves in a drug solution like hydrogen peroxide solution or a sulfuric acid, a TiN layer has the problem that the cleaning performed after etching of a gate electrode layer is very difficult. Therefore, the device of this structure was very difficult to maintain the yield highly.

[0008] Moreover, in N type or P-channel MOS FET, the following things can say in the gate electrode which has the tantalum layer formed on the gate insulating layer. the layer in which the tantalum layer had the beta phase which is quite high resistance (specific resistance: about 160micro ohm-cm) for a metal in this example of a configuration – membranes cannot be formed – as a result – comparatively – alike – quantity – there is a problem of becoming a gate electrode [****]. Moreover, in the case of this example of a configuration, it became and differed, the threshold has shifted to a low threshold side, and the intrinsic mid gap energy of silicon and the problem of NMOSFET and PMOSFET that threshold balance is bad have the work function of a beta tantalum layer.

[0009]

[Problem(s) to be Solved by the Invention] The purpose of this invention is to have high current drive capacity and for the yield offer a high semiconductor device and its manufacture approach.

[0010]

[Means for Solving the Problem] The 1st and 2nd impurity diffused layers which constitute the source field and drain field where the semiconductor device concerning this invention was formed in the semi-conductor layer, The channel field formed between said 1st and 2nd impurity diffused layers, The gate insulating layer formed on said channel field at least and the gate electrode formed on said gate insulating layer are included. Said gate electrode.The tantalum nitride layer formed in the field which touches said gate insulating layer at least, and the tantalum layer formed on this tantalum nitride layer are included.

[0011] According to the semiconductor device concerning this invention, it mainly has the following operation effectiveness.

[0012] (1) Said gate electrode has said tantalum nitride layer so that said gate insulating layer may be touched. That work function approximates this tantalum nitride layer extremely with the intrinsic mid GYAPU energy of silicon. Consequently, the increment in the absolute value of flat band voltage in the capacitor which consists of metal-insulating-layer-silicon is small, and does not have to make high concentration of the impurity doped by the channel field for control of a threshold. Therefore, the fall of carrier mobility can be prevented and the insulated-gate field-effect transistor equipped with high current drive capacity can be obtained by the high yield.

[0013] (2) As stated above (1), said tantalum nitride layer has the small increment in the absolute value of flat band voltage in the capacitor which consists of metal-insulating-layer-silicon since the work function approximates extremely with the intrinsic mid GYAPU energy of

silicon, and the difference of said absolute value can be made quite small in an N channel insulated-gate field-effect transistor and a P channel insulated-gate field-effect transistor. Consequently, in the complementary-type semiconductor device consolidated with an N channel insulated-gate field-effect transistor and a P channel insulated-gate field-effect transistor, both threshold balance is easily [correctly and] controllable. Especially this effectiveness is remarkable in the complementary-type semiconductor device which used SOI structure or SON structure.

[0014] (3) Since the polish recon layer is not in contact with a gate electrode including said tantalum nitride layer at least, said gate electrode does not produce depletion-ization in a gate electrode. Consequently, said gate electrode can make small reduction of the effectual electric field concerning a channel field compared with the case where a polish recon layer is used, and does not cause the fall of current drive capacity from this point, either.

[0015] (4) Compared with a titanium nitride layer etc., said tantalum nitride layer which constitutes said gate electrode has high chemical stability, for example, has the resistance which was excellent to the drug solution used for cleaning of a gate electrode. Consequently, a device can be manufactured by the high yield.

[0016] (5) Compared with said tantalum nitride layer, said tantalum layer which constitutes said gate electrode has small resistance, and can make conductivity of said gate electrode high. And said tantalum layer consists of tantalums of a body-centered cubic lattice phase preferably. The tantalum of a body-centered cubic lattice phase has high conductivity compared with a beta tantalum. Specifically, the tantalum of a body-centered cubic lattice phase can make resistance small to about 1/10 compared with a beta tantalum. Such a tantalum layer of a body-centered cubic lattice phase can be formed with hetero epitaxy growth by lattice matching with said tantalum nitride layer.

[0017] This invention can take the mode of further the following. These modes are the same also in the manufacture approach of of the complementary-type semiconductor device and semiconductor device which are mentioned later.

[0018] (A) If said tantalum nitride layer takes conductivity and a work function into consideration, the presentation ratios (x) of nitrogen and a tantalum expressed with TaNx can be 0.25-1.0. The presentation ratio (x) of nitrogen and a tantalum to which said especially tantalum nitride layer is expressed with TaNx can be about 0.5.

[0019] (B) Said tantalum nitride layer can have more preferably 1-50nm of 3-20nm thickness, if hetero epitaxy growth of a tantalum layer etc. is taken into consideration.

[0020] (C) Said gate electrode can have the cap layer which turns into the maximum upper layer from the oxidation-resistant quality of the material. Said cap layer can consist of TaNx, TaSixNy, TiNx, TiAlxNy, Si, and an ingredient that consists of at least one sort chosen from the silicide of transition metals. When said cap layer is a tantalum nitride layer, it is easy to form continuously each class which constitutes a gate electrode using the same equipment (for example, sputtering system), and it is advantageous at this point.

[0021] (D) In the outcrop of said impurity diffused layer, and a pan, it can have a silicide layer in the upper part of said gate electrode. In such a silicide layer existing, the conductivity of an impurity diffused layer and a gate electrode increases.

[0022] (E) Said semi-conductor layer can be SOI structure or SON structure. Furthermore, said semi-conductor layer may be the silicon layer with thickness small [including a very low-concentration impurity] formed on the semi-conductor substrate containing the impurity of high concentration, or a bulk half conductor layer.

[0023] This invention is applied suitable for a complementary-type semiconductor device, as mentioned above. Namely, the complementary-type semiconductor device concerning this invention An N channel insulated-gate field-effect transistor and a P channel insulated-gate field-effect transistor are loaded together. Each of said N channel insulated-gate field-effect

transistor and a P channel insulated-gate field-effect transistor The 1st and 2nd impurity diffused layers which constitute the source field or drain field formed in the semi-conductor layer, The channel field formed between said 1st and 2nd impurity diffused layers, Said gate electrode contains the tantalum nitride layer formed in the field which touches said gate insulating layer at least, and the tantalum layer formed on this tantalum nitride layer including the gate insulating layer formed on said channel field, and the gate electrode formed on said gate insulating layer.
[0024] According to this complementary-type semiconductor device, as mentioned above, since that work function approximates the tantalum nitride layer extremely with the intrinsic mid GYAPU energy of silicon, it can control correctly and easily the threshold balance of an N channel insulated-gate field-effect transistor and a P channel insulated-gate field-effect transistor. Especially this effectiveness is remarkable in the complementary-type semiconductor device which used SOI structure or SON structure.
[0025] The manufacture approach of the semiconductor device concerning this invention contains following process (a) - (c).
[0026] (a) the process which forms a gate insulating layer on a semi-conductor layer, and (b) – the process which is a process which forms a gate electrode on said gate insulating layer, forms a tantalum nitride layer in the field which touches said gate insulating layer at least, and forms a tantalum layer on this tantalum nitride layer further, and (c) – the process which forms the 1st and 2nd impurity diffused layers which introduce an impurity into said semi-conductor layer, and constitute a source field and a drain field.
[0027] And as mentioned above, said tantalum layer consists of tantalums of a body-centered cubic lattice phase preferably. The tantalum of a body-centered cubic lattice phase has high conductivity compared with a beta tantalum. Such a tantalum layer of a body-centered cubic lattice phase can be formed with hetero epitaxy growth by lattice matching with said tantalum nitride layer.
[0028] The manufacture approach of this invention can take the mode of further the following. These modes are the same also in the manufacture approach of the complementary-type semiconductor device mentioned later.
[0029] (A) In said process (c), said impurity diffused layer can be formed by the self aryne by using said gate electrode as a mask.
[0030] (B) The process (e) by which a sidewall spacer is formed on the side of said gate electrode after said process (c) can be included.
[0031] (C) After said process (e), a silicide layer can be formed at the outcrop of said impurity diffused layer.
[0032] (D) In said process (b), said tantalum nitride layer and said tantalum layer can be formed of sputtering. And said tantalum layer can take more certainly the crystal structure of a body-centered cubic lattice phase by said sputtering being performed under existence of a xenon or krypton gas. Furthermore, said process (a) and (b) do not have ********** in atmospheric air, and a processed object can be performed continuously.
[0033] Furthermore, the manufacture approach of a complementary-type semiconductor device that the N channel insulated-gate field-effect transistor concerning this invention and the P channel insulated-gate field-effect transistor were loaded together contains following process (a) - (c).
[0034] (a) They are the process which forms a gate insulating layer on a semi-conductor layer, and the process which forms a gate electrode on the (b) aforementioned gate insulating layer. An impurity is introduced into the process which forms a tantalum nitride layer in the field which touches said gate insulating layer at least, and forms a tantalum layer on this tantalum nitride layer further, and the (c) aforementioned semi-conductor layer. Are the process which forms a source field and a drain field, and the 1st and 2nd impurity diffused layers of the N type for said

N channel insulated-gate field-effect transistor are formed. The process which forms the 1st and 2nd impurity diffused layers of the P type for said P channel insulated-gate field-effect transistor.

[0035]

[Embodiment of the Invention] Next, the gestalt of operation of this invention is explained with reference to a drawing.

[0036] [The gestalt of the 1st operation]

(Device) Drawing 1 is the sectional view showing typically the semiconductor device 1000 concerning the gestalt of operation of the 1st of this invention. A semiconductor device 1000 is a semiconductor device of a CMOS mold, and contains N channel insulated-gate field-effect transistor (NMOSFET) 100A and P channel insulated-gate field-effect transistor (PMOSFET) 100B. NMOSFET100A and PMOSFET100B are formed in the SOI (Silicon On Insulator) substrate 1. On support substrate 1c, the laminating of insulating-layer (silicon oxide layer) 1b and the low-concentration P type silicon layer 1a is carried out, and the SOI substrate 1 is constituted. And NMOSFET100A and PMOSFET100B are electrically separated by the slot 20 formed in P type silicon layer 1a of the SOI substrate 1, respectively.

[0037] Each MOSFETs 100A and 100B have the structure where the gate electrode 3 of a laminating mold was formed through the gate insulating layer 2 on P type silicon layer 1a. The laminating of the tantalum nitride layer 4, the tantalum layer 5 of a body-centered cubic lattice phase, and the tantalum nitride layer 6 as a cap layer is carried out one by one, and this laminating type of gate electrode 3 is constituted. Moreover, directly under the gate insulating layer 2, the impurity diffusion fields 8a and 8b which constitute a source drain field (a source field or drain field) are established in the both ends of the channel field 7 and the channel field 7.

[0038] And in NMOSFET100A, impurity diffused layers 8a and 8b are formed in N type, and impurity diffused layers 8a and 8b are formed in P type by PMOSFET100B. The silicide layers 10a and 10b are formed in the upper part of impurity diffused layers 8a and 8b, respectively.

[0039] The tantalum nitride layer 4 is formed in the field which touches the gate insulating layer 2 at least in the gestalt of this operation. Moreover, when points, such as conductivity and a threshold property, are taken into consideration, as for the tantalum nitride layer 4, it is desirable for the presentation ratios (x) of nitrogen and a tantalum expressed with TaNx to be 0.25-1.0. When the gate electrode 3 is a laminated structure and the crystal growth of the tantalum layer 5 is especially taken into consideration, as for the tantalum nitride layer 4, it is desirable for the presentation ratio (x) of nitrogen and a tantalum expressed with TaNx to be about 0.5.

[0040] Furthermore, the gate electrode 3 can prevent that the tantalum layer 5 receives a damage by oxidization to an acid chemically-modified [next] degree by having the tantalum nitride layer 6 as a cap layer which turns into the maximum upper layer from the oxidation-resistant quality of the material. The quality of the material which consists of at least one sort chosen from TaNx, TaSixNy, TiNx, TiAlxNy, Si, the silicide of transition metals, etc. can constitute such a cap layer.

[0041] According to the semiconductor device concerning the gestalt of this operation, it mainly has the following operation effectiveness.

[0042] (1) The gate electrode 3 has the tantalum nitride layer 4 so that the gate insulating layer 2 may be touched. That work function is about 4.5eV, and approximates this tantalum nitride layer 4 extremely with intrinsic mid GYAPU energy 4.61eV of silicon. Consequently, the increment in the absolute value of flat band voltage in an MOS capacitor is small, and does not have to make high concentration of the impurity doped by the channel field for control of a threshold. Therefore, the fall of carrier mobility can be prevented and MOSFET equipped with high current drive capacity can be obtained by the high yield.

[0043] (2) As stated above (1), since the work function approximates the tantalum nitride layer 4 extremely with the intrinsic mid GYAPU energy of silicon, its increment in the absolute value of flat band voltage in an MOS capacitor is small, and the difference of said absolute value can be made quite small in NMOSFET and PMOSFET. Consequently, in CMOS consolidated with NMOSFET and PMOSFET, both threshold balance is easily [correctly and] controllable. Especially this effectiveness is remarkable in CMOS which used the SOI substrate.
[0044] (3) Since it consists of the tantalum nitride layer 4, a tantalum layer 5, and a tantalum nitride layer 6 and the polish recon layer is not in contact with a gate electrode, the gate electrode 3 does not produce depletion-ization in a gate electrode. Consequently, the gate electrode 3 can make small reduction of the effectual electric field concerning a channel field compared with the case where a polish recon layer is used, and does not cause the fall of current drive capacity from this point, either.
[0045] (4) All, compared with a titanium nitride layer etc., the tantalum nitride layer 4 and the tantalum layer 5 which constitute the gate electrode 3 have high chemical stability, for example, have the resistance which was excellent to the drug solution used for cleaning of a gate electrode. Consequently, a device can be manufactured by the high yield.
[0046] (5) Since the tantalum layer 5 which constitutes the gate electrode 3 consists of tantalums of a body-centered cubic lattice phase, compared with a beta tantalum, its conductivity is high. Specifically, the tantalum of a body-centered cubic lattice phase can make resistance small to about 1/10 compared with a beta tantalum.
[0047] In this invention, creation explains the characteristic test of a device in full detail behind in formation of the difficult tantalum of a body-centered cubic lattice phase, and a list conventionally.
[0048] (The manufacture approach) The manufacture approach of a semiconductor device 1000 is explained with reference to drawing 2 - drawing 5 .
[0049] (a) First, as shown in drawing 2 , carry out patterning of the P type silicon layer 1a of 50nm in thickness, specific resistance 14 - 26 ohm-cm, and field bearing (100), and form the slot 20 for isolation.
[0050] (b) Subsequently, as shown in drawing 3 , form the gate insulating layer 2 which consists of a silicon oxide layer of about 3nm of thickness by the oxidizing [thermally] method.

[0051] Furthermore, the tantalum nitride layer 4, the tantalum layer 5 of a body-centered cubic lattice phase, and the tantalum nitride layer 6 as a cap layer are formed by sputtering using xenon gas, for example, reactive sputtering, one by one.
[0052] In sputtering, it becomes possible to give energy only to the front face of the layer under membrane formation, without giving a defect or a damage to the gate insulating layer 2 of a substrate, and silicon layer 1a by using a xenon with more large mass instead of the argon usually used. That is, to the atomic radius of an argon being 0.188nm, the atomic radius of a xenon is as large as 0.217nm, cannot advance easily into a layer, and can give energy efficiently only on the surface of a layer. And the atomic weight of an argon is 39.95, the atomic weight of a xenon is 131.3 and atomic weight of a xenon is large compared with an argon. Therefore, it can be said that the energy to a layer and the transmission efficiency of a xenon of momentum are low compared with an argon, and it is hard to make a defect and a damage. Therefore, a xenon can form the tantalum nitride layer 4 and the tantalum layer 5 without giving a defect and a damage to a gate insulating layer compared with an argon. This inclination can be said also about a krypton.
[0053] adopting the membrane formation approach mentioned above in the gestalt of this operation -- it is -- low -- it was checked that the tantalum layer [****] 5 of a body-centered cubic lattice phase can form by hetero epitaxy growth by lattice matching on the tantalum nitride layer 4. When hetero epitaxy growth of the tantalum layer 5, the conductivity of the gate

electrode 3, etc. are taken into consideration, as for the thickness, it is [the tantalum nitride layer 4] desirable that it is 1-50nm. Moreover, the upper tantalum nitride layer 6 has a function as a cap layer which prevents oxidation in the process after etching of a gate electrode.
[0054] Furthermore, as for these tantalum nitride layers 4, the tantalum layer 5 of a body-centered cubic lattice phase, and the tantalum nitride layer 6, being formed continuously is desirable, without being exposed to atmospheric air. If the film is exposed to atmospheric air in the middle of membrane formation, moisture carries out a miscarriage, or an oxide is formed on the surface of the film, and it is not desirable.
[0055] Next, a lithography technique and a dry etching technique perform patterning of a gate electrode.
[0056] (c) Subsequently, as shown in drawing 4 , carry out the ion implantation of the 2 boron-fluoride ion (BF2+) for arsenic ion (As+) to PMOSFET by three or more [1020cm -] concentration by using the gate electrode 3 as a mask at NMOSFET. In case the impurity diffused layer of NMOSFET and PMOSFET is formed, mask layers (not shown), such as a resist layer, are formed in a predetermined field so that the impurity ion of reversed polarity may not be doped.
[0057] Then, 700 degrees C or less of impurity diffused layers 8a and 8b can be formed by the self aryne by giving 450-550-degree C low-temperature annealing preferably.
[0058] next, CVD (Chemical Vapor Deposition) – in law, after depositing a silicon oxide layer extensively on the SOI substrate 1 with which the gate electrode 3 was formed, etchback is performed by the dry etching method and the sidewall spacer 9 is formed.
[0059] Furthermore, a transition-metals layer, for example, nickel layer, is formed in a spatter, and the nickel silicide layers 10a and 10b are formed in the outcrop of impurity diffused layers 8a and 8b through annealing. As such transition metals, titanium (Ti), cobalt (Co), etc. just make silicide. Then, acids, such as a sulfuric acid, remove the unreacted transition-metals layer on a sidewall 9, and the silicide layers 10a and 10b are formed by the self aryne.
[0060] (d) After this, by passing through the wiring process by the usual CMOS process technique, the layer insulation layer 12 and a wiring layer 13 can be formed, and a semiconductor device 1000 can be completed.
[0061] According to the above manufacture approach, five layers of tantalums of a body-centered cubic lattice phase can be formed by hetero epitaxy on said tantalum nitride layer 4 with sputtering by forming the tantalum nitride layer 4 in the field which touches the gate insulating layer 2 at least.
[0062] (The crystal structure and characteristic test) The various characteristic tests for which it asked about the semiconductor device for the semiconductor device concerning this invention and a comparison are hereafter stated to the hetero epitaxy technique by the crystal structure of the semiconductor device concerning this invention, i.e., the lattice matching of a gate electrode, and a list. The sample used for the analysis and the characteristic test of the crystal structure is as follows.
[0063] Sample of this invention ;P The CMOS mold semiconductor device is formed in the SOI substrate 1 whose thickness of mold silicon layer 1a is 57nm. And the gate insulating layer 2 consists of 3.8nm of thickness, and a 5.5nm silicon oxide layer, and a CMOS mold semiconductor device has the tantalum nitride layer 4 of 5nm of thickness by which the gate electrode 3 was formed on the gate insulating layer 2, and the tantalum layer 5 of the body-centered cubic lattice phase of 158nm of thickness. Moreover, as a sample for asking for the capacitance of MOS, the silicon oxide layer of 11.5nm of thickness was prepared instead of the above-mentioned gate insulating layer on the bulk layer which consists of P type silicon, and what has the tantalum nitride layer which has the same thickness as the above-mentioned gate electrode on this silicon oxide layer, and the tantalum layer of a body-centered cubic lattice phase was used.

[0064] The sample for a comparison; a gate electrode does not have a tantalum nitride layer in the sample of this invention, and consists of beta tantalum layers, and also it has the same configuration as the sample of this invention.
[0065] (1) Crystal structure drawing 6 shows the diffraction peak of the tantalum layer in the sample and the sample for a comparison of this invention by the X-ray diffraction method. In drawing 6 , as for an axis of ordinate, an axis of abscissa shows reinforcement for whenever [angle-of-diffraction]. In drawing 6 , the graph shown with Sign a is as a result of the sample concerning this invention, and the graph shown with Sign b shows the result of the sample for a comparison.
[0066] ****** to which the alpha tantalum of the body-centered cubic lattice phase (bcc) of low resistance grows, and the beta tantalum is not growing from drawing 6 on a tantalum nitride layer by the sample of this invention to the beta tantalum of high resistance growing with the sample for a comparison on SiO two-layer (gate insulating layer) – things are understood.
[0067] From this, growth of a tantalum layer is considered to be influenced by the layer of a substrate. Whenever [lattice constant / of a tantalum and tantalum nitride / (d), field bearing (hkl), and angle-of-diffraction] (2theta) is shown in Table 1. Table 1 shows that the field (110) of the alpha tantalum (bcc-Ta) of a body-centered cubic lattice phase and the field (101) of nitriding 2 tantalum (TaN0.5) have the very near lattice constant. The mismatch of both lattice constant is about only 0.68%.
[0068]
[Table 1]
【表1】

	(hkl)	d (nm)	2θ (deg)
β−Ta	(002)	0.2658	33.69
β−Ta	(410)	0.2474	33.28
β−Ta	(202)	0.2354	38.20
bcc−Ta	(110)	0.2338	38.47
Ta_2N	(101)	0.2323	38.73
TaN	(200)	0.2169	41.60

When the interface of tantalum nitride and the alpha tantalum formed on it was checked by the cross-section observation by the transmission electron microscope, it actually became clear that both of the layers had the almost same lattice constant of about 0.23nm as the value shown in Table 1. The cross-section photograph by the transmission electron microscope is shown in drawing 7 :
[0069] From the above thing, it was checked with the sample of this invention that the alpha tantalum (bcc-Ta) of a body-centered cubic lattice phase carries out hetero epitaxy growth by lattice matching on tantalum nitride (TaN0.5). On the other hand, with the sample for a comparison, it was checked that the beta tantalum layer is formed on a gate insulating layer (silicon oxide layer).
[0070] (2) The order SUTATEKKU C-V property was searched for about the sample and the sample for a comparison of semi- SUTATEKKU (Quasi-Static) C-V property this invention. The result is shown in drawing 8 . In drawing 8 , an axis of abscissa shows gate voltage and an axis of ordinate shows capacitance. Moreover, in drawing 8 , the graph shown with Sign a is as a result of the sample concerning this invention, and the graph shown with Sign b shows the result of the sample for a comparison.
[0071] As for drawing 8 , since the value of a capacitor wardrobe is symmetrical to the 1st negative [of gate voltage / forward and negative], both samples show that depletion-ization has not taken place to a gate electrode the 1st. On the whole, the sample of this invention has [2nd] a low capacitor wardrobe compared with the sample for a comparison. This shows that the reaction layer to which a beta tantalum and a gate insulating layer react, and a capacitor

wardrobe becomes large is formed in the sample for a comparison. Therefore, with the sample of this invention, it turns out that it had chemical stability with a gate electrode, especially a tantalum nitride layer higher than the sample for a comparison, and the rise of a capacitor wardrobe is controlled.
[0072] (3) It asked for the barrier height of the electron in the interface of the gate electrode and gate insulating layer to the gas mixture rate (nitrogen/(xenon + nitrogen)) of the nitrogen when forming the tantalum nitride layer which constitutes the barrier height gate electrode of the electron in the interface of a gate electrode (tantalum nitride layer) and a gate insulating layer by sputtering. In drawing 9 , Sign a shows the result. In drawing 9 , an axis of abscissa shows a gas mixture rate, and an axis of ordinate shows electronic barrier height.
[0073] Electronic barrier height also becomes large and a mixed rate becomes almost fixed [the value] from the graph a of drawing 9 by about 1 volume % as the rate of the nitrogen at the time of sputtering becomes large. From this graph a, by making the mixed rate of nitrogen gas increase to 1 volume % extent at least shows that the work function of a tantalum nitride layer becomes large.
[0074] (4) About the sample and the sample for a comparison of gate length-threshold voltage characteristic this invention, change of the threshold electrical potential difference to gate length was investigated. The result is shown in drawing 10 R> 0. In drawing 10 , an axis of abscissa shows gate length and an axis of ordinate shows a threshold electrical potential difference. In drawing 10 , signs a1 and a2 show the result of the sample of this invention, and signs b1 and b2 show the result of the sample for a comparison. Moreover, signs a1 and b1 show the result of NMOSFET, and signs a2 and b2 show the result of PMOSFET.
[0075] Drawing 10 shows that a threshold electrical potential difference rises on the whole by both NMOSFET and PMOSFET, and the symmetric property over threshold electrical-potential-difference zero is improved compared with the sample for a comparison with the sample of this invention. This shows that the work function of a tantalum nitride layer approximates with the mid gap energy of silicon compared with it of a beta tantalum layer.
[0076] The semiconductor device 2000 concerning the gestalt of the 2nd operation of [gestalt of the 2nd operation] this invention and its manufacture approach are explained with reference to drawing 11 - drawing 14 . The gestalten of this operation differ in that the cap layer the gestalt of the 1st operation and for the anti-oxidation of a gate electrode consists of silicide layers 15 of an amorphous substance or a polycrystalline silicon layer instead of the tantalum nitride layer. About a semiconductor device 2000, the same sign is substantially given to the same part with the semiconductor device 1000 concerning the gestalt of the 1st operation, and the detailed explanation is omitted.
[0077] That is, the gate electrode 3 is constituted from the silicide layer 15 of the tantalum nitride layer 4 which touches the gate insulating layer 2, the tantalum layer 5 of a body-centered cubic lattice phase and an amorphous substance, or a polycrystalline silicon layer by the gestalt of this operation.
[0078] In addition to the operation effectiveness which the semiconductor device 1000 of the gestalt of the 1st operation has, the semiconductor device 2000 of the gestalt of this operation has the following operation effectiveness. That is, according to the semiconductor device 2000, the conductivity of the gate electrode 3 becomes higher with a cap layer consisting of silicide layers 15.
[0079] (The manufacture approach) The manufacture approach of a semiconductor device 2000 is explained with reference to drawing 11 - drawing 14 .
[0080] (a) First, as shown in drawing 11 , carry out patterning of the P type silicon layer 1a of 50nm in thickness, specific resistance 14 - 26 ohm-cm, and field bearing (100), and form the slot 20 for isolation.
[0081] (b) Subsequently, as shown in drawing 12 , form the gate insulating layer 2 which

consists of a silicon oxide layer of about 3nm of thickness by the oxidizing [thermally] method.

[0082] Furthermore, the tantalum nitride layer 4, the tantalum layer 5 of a body-centered cubic lattice phase, and amorphous or the silicon layer 14 of polycrystal is formed by the sputtering method using xenon gas, for example, reactive sputtering, one by one.
[0083] In sputtering, it becomes possible like the gestalt of the 1st operation to give energy only to the front face of the layer under membrane formation instead of the argon usually used, without giving a defect or a damage to the gate insulating layer 2 of a substrate, and silicon layer 1a by using a xenon with more large mass.
[0084] Furthermore, as for amorphous or the silicon layer 14 of polycrystal, it is desirable these tantalum nitride layers 4, the tantalum layer 5 of a body-centered cubic lattice phase, and to be formed continuously, without being exposed to atmospheric air. If the film is exposed to atmospheric air in the middle of membrane formation, moisture carries out a miscarriage, or an oxide is formed on the surface of the film, and it is not desirable.
[0085] low – the tantalum layer [****] 5 of a body-centered cubic lattice phase carries out hetero epitaxy growth by lattice matching on the tantalum nitride layer 4 like the gestalt of the 1st operation. Moreover, the upper silicon layer 14 is silicide-ized in a next process, and has a function as a cap layer which finally prevents oxidation of the tantalum layer 5.
[0086] Next, a lithography technique and a dry etching technique perform patterning of a gate electrode.
[0087] (c) Subsequently, as shown in drawing 13 , carry out the ion implantation of the 2 boron-fluoride ion (BF2+) for arsenic ion (A s+) to PMOSFET by three or more [1020cm -] concentration by using the gate electrode 3 as a mask at NMOSFET. In case the impurity diffused layer of NMOSFET and PMOSFET is formed, mask layers (not shown), such as a resist layer, are formed in a predetermined field so that the impurity ion of reversed polarity may not be doped.
[0088] Then, 700 degrees C or less of impurity diffused layers 8a and 8b can be formed by the self aryne by giving 450-550-degree C low-temperature annealing preferably. next, CVD (Chemical Vapor Deposition) – in law, after depositing a silicon oxide layer extensively on the SOI substrate 1 with which the gate electrode 3 was formed, etchback is performed by the dry etching method and the sidewall spacer 9 is formed.
[0089] Furthermore, a transition-metals layer, for example, nickel layer, is formed in a spatter, and the nickel silicide layers 10a and 10b and 15 are formed in the outcrop of impurity diffused layers 8a and 8b and the silicon layer 14 through annealing. Then, acids, such as a sulfuric acid, remove the unreacted transition-metals layer on a sidewall 9, and the silicide layers 10a, 10b, and 15 are formed by the self aryne.
[0090] (d) After this, by passing through the wiring process by the usual CMOS process technique, the layer insulation layer 12 and a wiring layer 13 can be formed, and a semiconductor device 2000 can be completed.
[0091] As mentioned above, although the gestalt of the suitable operation for this invention was described, this invention can take various kinds of modes by within the limits of the summary.

[Translation done.]